

## **CLAIM AMENDMENTS**

### **Claim Amendment Summary**

#### **Claims pending**

- Before this Amendment: Claims 1-7, 10-30, and 32-35
- After this Amendment: Claims 1-7, 10-30, and 32-35

**Non-Elected, Canceled, or Withdrawn claims:** None

**Amended claims:** 1, 4, 10, 11, 14, 16, 20, 22, 24, 27, 32, 33, and 35

**New claims:** None

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### **Claims:**

1. (Currently Amended) A digital storage system storing data, the data including a coded binary sequence having:

a first group of at least six consecutive bits, the first group having first and second separate portions and representing one of a logic 1 and a logic 0, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of at least six consecutive bits separate from the first group and each having the first state, the second group representing only the other of the logic 1 and the logic 0.

2. (Previously Presented) The storage system of claim 1 wherein the first and second portions of the first group respectively comprise first and second halves of the first group.

3. (Previously Presented) The storage system of claim 1 wherein the first and second groups respectively represent logic 1 and logic 0, and the first and second states respectively equal logic 0 and logic 1.

4. (Currently Amended) A digital storage system storing data, the data including a coded binary sequence having:

a first group of at least six consecutive bits each having a first state, the first group representing only one of a logic 1 and a logic 0; and

a second group of at least six consecutive bits separate from the first group, the second group having first and second separate portions and representing the other of the logic 1 and the logic 0, the bits in the first portion each having the first state and the bits in the second portion each having a second state.

5. (Previously Presented) The storage system of claim 4 wherein:  
the first and second groups respectively represent logic 0 and logic 1;  
and  
the first and second states respectively equal logic 0 and logic 1.

6. (Previously Presented) The storage system of claim 4 wherein the first and second groups each respectively comprise four consecutive bits.

7. (Previously Presented) The storage system of claim 4 wherein the first and second portions of the second group respectively comprises first and second halves of the second group.

8-9. (Canceled)

10. (Currently Amended) A storage disk, comprising:  
disk sectors operable to store application data; and  
servo wedges that store servo data that includes,

a first group of at least six consecutive bits, the first group having first and second nonoverlapping portions and representing one of a logic 1 and a logic 0, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of at least six consecutive bits separate from the first group and each having the first state, the second group representing only the other of the logic 1 and the logic 0.

11. (Currently Amended) A Viterbi detector, comprising:

an input node operable to receive a signal that represents a binary sequence having a first group of at least six consecutive bits each having a first logic level and a second group of at least six consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing only the first logic level and the second group representing the second logic level; and

a circuit coupled to the input node and operable to recover the binary sequence from the signal.

12. (Original) The Viterbi detector of claim 11 wherein the binary sequence comprises a coded binary sequence.

13. (Original) The Viterbi detector of claim 11 wherein:

the first logic level comprises a logic 0; and

the second logic level comprises a logic 1.

14. (Currently Amended) A servo circuit, comprising:

a sample circuit operable to generate samples of a signal that represents a coded binary sequence having a first group of at least six consecutive bits each having a first logic level and a second group of at least six consecutive bits, the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing only the first logic level and the second group representing the second logic level; and

a Viterbi detector coupled to the sample circuit and operable to recover the coded binary sequence from the samples of the signal.

15. (Original) The servo circuit of claim 14, further comprising a decoder coupled to the Viterbi detector and operable to decode the recovered binary sequence.

16. (Currently Amended) A disk-drive system, comprising:

a data-storage disk having a surface, data sectors at respective locations of the surface, and servo wedges that store servo data that includes a first group of at least six consecutive bits each having a first logic level and a second group at least six consecutive bits having first and second portions of consecutive bits, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level, the first group representing only the first logic level and the second group representing the second logic level;

a motor coupled to and operable to rotate the disk;

a read head operable to generate a servo signal that represents the servo data and having a position with respect to the surface of the data-storage disk;

a read-head positioning circuit operable to move the read head over the surface of the disk; and

a servo circuit coupled to the read head and operable to recover the servo data from the servo signal.

17. (Original) The disk-drive system of claim 16 wherein the servo circuit comprises: a sample circuit operable to generate samples of the servo signal; and

a Viterbi detector coupled to the sample circuit and operable to recover the servo data from the samples of the servo signal.

18. (Original) The disk-drive system of claim 16 wherein the servo circuit comprises a decoder operable to decode the recovered servo data.

19. (Original) The disk-drive system of claim 16 wherein the read head comprises a read-write head.

20. (Currently Amended) A method, comprising:  
coding one of a logic 1 and a logic 0 as a first group of at least six consecutive bits, the first group having first and second equally sized portions, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and  
coding the other and only the other of the logic 1 and the logic 0 as a second group of at least six consecutive bits separate from the first group and each having the first state.

21. (Previously Presented) The method of claim 20 wherein the first and second groups respectively represent a logic 1 and a logic 0, and the first and second states respectively equal logic 0 and logic 1.

22. (Currently Amended) The method of claim 20 wherein the coding comprises:

coding the one of the logic 1 and the logic 0 as a first group of ~~[[four]]~~eight consecutive bits; and

coding the other of the logic 1 and the logic 0 as a second group of ~~[[four]]~~eight consecutive bits.

23. (Previously Presented) The method of claim 20 wherein the first and second portions of the first group respectively comprise first and second halves of the first group.

24. (Currently Amended) A method, comprising:

coding a first logical bit of servo data and only the first logical bit as a first group of ~~[[four]]~~eight consecutive bits each having a first logic level, the first logical bit representing the first or a second logic level; and

coding a second logical bit of servo data as a second group of ~~[[four]]~~eight consecutive bits respectively having the first logic level, the first logic level, the second logic level, and the second logic level, the second logical bit representing the first logic level if the first logical bit represents the second logic level, the second logical bit representing the second logic level if the first logical bit represents the first logic level.

25. (Previously Presented) The method of claim 24 wherein:

the first logical bit equals a logic 0; and

the second logical bit equals a logic 1.

26. (Original) The method of claim 24 wherein:  
the first logic level equals a logic 0; and  
the second logic level equals a logic 1.

27. (Currently Amended) A method, comprising:  
writing a first code symbol into a servo wedge of a data-storage disk,  
the first code symbol having a first group of at least six code bits and a second  
group of at least six code bits, having a length, and representing one of a logic 1  
and a logic 0, each bit in the first group having a first value and each bit in the  
second group having a second value that is different than the first value; and  
writing a second code symbol into the servo wedge, the second  
code symbol having the length or approximately the length, having a single group  
of code bits each having the first value, and representing only the other of the  
logic 1 and the logic 0.

28. (Previously Presented) The method of claim 27 wherein:  
the first and second code symbols each comprise a first number of  
bits;  
the servo wedge comprises a second number of bits; and  
the lengths of the first and second code symbols are each less than  
the product of the first and second numbers.

29. (Original) The method of claim 27 wherein:  
the first code symbol represents a logic 0; and  
the second code symbol represents a logic 1.

30. (Previously Presented) The method of claim 27 wherein each of the first and second groups of code bits is or is approximately half as long as the first code symbol.

31. (Canceled)

32. (Currently Amended) A digital storage system, comprising servo data that includes:

a first group of at least six consecutive bits, the first group having first and second portions and representing one of a logic 1 and a logic 0, the first portion preceding the second portion, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of at least six consecutive bits each having the first state, the second group representing only the other of the logic 1 and the logic 0.

33. (Currently Amended) A digital storage system, comprising servo data that includes:

a first group of at least six consecutive bits, the first group having first and second portions and representing one of a logic 1 and a logic 0, the first portion preceding the second portion, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of at least six consecutive bits, the second group representing only the other of the logic 1 and the logic 0, all of the bits of the second group having the first state or all of the bits of the second group having the second state.

34. (Previously Presented) The disk storage servo wedge of claim 33 wherein:

the first group represents a logic 1;



the first state comprises a logic 0;  
the second state comprises a logic 1;  
each bit of the second group has the first state; and  
the second group represents a logic 0.

35. (Currently Amended) A digital storage system storing data, the data including a coded binary sequence having:

a first group of at least six consecutive bits, the first group having first and second separate portions and representing one of a logic 1 and a logic 0, the bits in the first portion each having a first state and the bits in the second portion each having a second state; and

a second group of at least six consecutive bits separate from the first group and each having the second state, the second group representing only the other of the logic 1 and the logic 0; wherein the second state is a binary '1'.